

CLAIMS:

What is claimed is:

1 1. A method of processing a multiplication operation instruction, comprising:  
2 fetching and decoding a multiplication operation instruction;  
3 executing the multiplication operation instruction on a multiplication source operand to  
4 generate a square of the multiplication source operand, the multiplication source operand  
5 contained in a multiplication operand source register specified in the multiplication operation  
6 instruction; and

7 storing a result output in a target accumulator specified in the multiplication operation  
8 instruction;

9 wherein the multiplication source operand is transferred directly from the multiplication  
10 operand source register to a multiplication execution unit for immediate generation of the square  
11 output for the multiplication source operand.

12 2. The method according to claim 1, wherein the step of executing the multiplication  
1 operation instruction includes the step of generating a difference output between a minuend  
2 source operand and a subtrahend source operand.

3 3. The method according to claim 2, wherein the step of executing the multiplication  
1 operation instruction includes the step of storing the difference output in a difference register  
2 specified in the multiplication operation instruction.

1 4. The method according to claim 3, wherein the minuend source operand and the  
2 subtrahend source operand are fetched during execution of a preceding multiplication operation  
3 instruction.

1 5. The method according to claim 4, wherein the multiplication operation instruction  
2 specifies a first source register, the first source register containing an address for the minuend  
3 source operand, wherein the minuend source operand is transferred directly from the address to  
4 an arithmetic execution unit for immediate generation of the difference output.

6. The method according to claim 5, wherein the multiplication operation instruction  
specifies a second source register, the second source register containing an address for the  
subtrahend source operand, wherein the subtrahend source operand is transferred directly from  
the address to an arithmetic execution unit for immediate generation of the difference output.

7. The method according to claim 6, wherein the multiplication operation instruction is a  
Euclidean Distance operation.

1 8. The method according to claim 7, wherein the result output is the square of the  
2 multiplication source operand.

1 9. The method according to claim 6, wherein the multiplication operation instruction is an  
2 Euclidean Distance Accumulate operation.

1 10. The method according to claim 9, wherein the step of executing the multiplication  
2 operation instruction includes the step of adding the square of the multiplication source operand  
3 to an addition source operand, the addition source operand contained in the target accumulator  
4 specified in the multiplication operation instruction.

1 11. The method according to claim 10, wherein the result output is the sum of the square of  
2 the multiplication source operand and the addition source operand.

1 12. The method according to claim 10, wherein the step of executing the multiplication  
2 operation instruction includes modifying the address contained in the first source register to  
3 contain an address for a next minuend operand for computing a difference during execution of a  
4 subsequent multiplication operation instruction.

1 13. The method according to claim 12, wherein the step of executing the multiplication  
2 operation instruction includes modifying the address contained in the second source register to  
3 contain an address for a next subtrahend operand for computing the difference during execution  
4 of the subsequent multiplication operation instruction.

1 14. The method according to claim 1, further comprising:  
2 setting an accumulator status flag.

1 15. A processor for multiplication operation instruction processing, comprising:

2 a program memory for storing instructions including a multiplication operation

3 instruction;

4 a program counter for identifying current instructions for processing; and

5 a Digital Signal Processing unit (DSP) for executing instructions within the program  
6 memory, the DSP including DSP logic for executing the multiplication operation instruction on a  
7 multiplication source operand to generate a square of the multiplication source operand, the  
8 multiplication source operand contained in a multiplication source operand register specified in  
9 the multiplication operation instruction; and

10 a target accumulator for storing a result output, the target accumulator specified in the  
11 multiplication operation instruction;

12 wherein the multiplication source operand is transferred directly from the multiplication  
13 operand register to a multiplication execution unit for immediate generation of the square of the  
14 multiplication source operand.

15 16. The processor according to claim 15, further comprising an arithmetic logic unit (ALU)  
16 for executing the instructions within program memory, the ALU including ALU logic for  
17 executing the multiplication operation instruction on a minuend source operand and a  
18 subtrahend source operand to generate a difference output.

1 17. The processor according to claim 16, further comprising the ALU storing the difference  
2 output in a difference register specified in the multiplication operation instruction.

1 18. The processor according to claim 17, wherein the minuend source operand and the  
2 subtrahend source operand are fetched during execution of a preceding multiplication operation  
3 instruction.

1 19. The processor according to claim 18, further comprising a first source register containing  
2 the address of the minuend source operand, the first source register specified in the  
3 multiplication operation instruction, wherein the minuend source operand is transferred directly  
4 from the address to an arithmetic execution unit for immediate generation of the difference.

63 20. The processor according to claim 19, further comprising a second source register  
64 containing the address of the subtrahend source operand, the second source register specified in  
65 the multiplication operation instruction, wherein the subtrahend source operand is transferred  
66 directly from the address to an arithmetic execution unit for immediate generation of the  
67 difference.

68 21. The processor according to claim 20, wherein the multiplication operation instruction is  
69 an Euclidean Distance operation.

1 22. The processor according to claim 21, wherein the result output is the square of the  
2 multiplication source operand.

1 23. The processor according to claim 22, wherein the multiplication operation instruction is  
2 an Euclidean Distance Accumulate operation.

1 24. The processor according to claim 23, further comprising the ALU for adding an addition  
2 source operand to the square of the multiplication source operand, the addition source operand  
3 contained in the target accumulator specified in the multiplication operation instruction.

1 25. The processor according to claim 24, wherein the result output is the sum of the square of  
2 the multiplication source operand and the addition source operand.

1 26. The processor according to claim 15, further comprising the ALU for modifying the  
2 address contained in the first source register to contain an address for a next minuend operand for  
3 computing a difference during execution of a subsequent multiplication operation instruction.

4 27. The processor according to claim 26, further comprising the ALU for modifying the  
5 address contained in the second source register to contain an address for a next subtrahend  
6 operand for computing the difference during execution of the subsequent multiplication  
7 operation instruction.

1 28. The processor according to claim 15, further comprising:  
2 a status register for indicating accumulator status.